WHAT IS CLAIMED IS:

1. A semiconductor packaging structure comprising:

a metal lead frame having a die pad and having a plurality of leads arranged around the die pad, wherein the metal lead frame has multiple gaps and each gap is defined by an adjacent two of the plurality of leads, and the multiple gaps are filled with an isolating resin;

a wall portion formed on the metal lead frame and positioned along a periphery of the metal lead frame;

a chip mounted on the die pad of the metal lead frame and electrically connected to the plurality of leads; and

a cover mounted on the wall portion to enclose the chip inside the wall portion.

2. The semiconductor packaging structure as claimed in claim 1 further having multiple notches and each notch is defined on a bottom surface of the metal lead frame and is communicated with one of the multiple gaps, wherein each notch and gap are filled with the isolating resin.

3. The semiconductor packaging structure as claimed in claim 1, wherein the die pad is higher than of the plurality of leads, whereby a space is defined below the die pad to receiving the isolating pad.

4. The semiconductor packaging structure as claimed in claim 2, wherein the cover is a transparent cover.

5. The semiconductor packaging structure as claimed in claim 3, wherein the cover is a transparent cover.

6. The semiconductor packaging structure as claimed in claim 2, wherein

the cover is a metal cover.

7. The semiconductor packaging structure as claimed in claim 3, wherein the cover is a metal cover.

8. The semiconductor packaging structure as claimed in claim 4, wherein the wall portion is formed of the isolating resin, and the wall portion is integrally formed with the isolating resin that fills the multiple gaps.

9. The semiconductor packaging structure as claimed in claim 5, wherein the wall portion is formed of the isolating resin, and the wall portion is integrally formed with the isolating resin that fills the multiple gaps.

10. A semiconductor packaging structure comprising:

a metal lead frame composed of an upper lead frame and a lower lead frame, wherein

the upper lead frame has a first die pad, a first plurality of leads arranged around the first die pad, a first interval defined between the first die pad and the first plurality of leads, and a first plurality of gaps each is defined by an adjacent two of the first plurality of leads and is communicated with the first interval;

the lower lead frame has a second die pad, a second plurality of leads arranged around the second die pad, a second interval defined between the second die pad and the second plurality of leads, and a second plurality of gaps, each of the second plurality of gapsis defined by two adjacent of the second plurality of leads and is communicated with the second interval, wherein when the upper lead frame and the upper lead frame are compressed together, the first interval, the second interval, the

first and the second plurality of gaps are communicated with each other for receiving an isolating resin;

a wall portion formed around a periphery of the upper lead frame;

a chip mounted on the first die pad of the upper lead frame and electrically connected to the first plurality of leads; and

a cover mounted on the wall portion to enclose the chip inside the wall portion.

11. The semiconductor packaging structure as claimed in claim 10, wherein the second die pad is slightly smaller than the first die pad.

12. The semiconductor packaging structure as claimed in claim 10, wherein each of the first plurality of leads has an external portion extending toward a flange of the upper lead frame, and has an internal portion extending toward the first die pad, each of the second plurality of leads corresponds to the external portion of one of the first plurality of leads.

13. The semiconductor packaging structure as claimed in claim 11, wherein each of the first plurality of leads has an external portion extending toward a flange of the upper lead frame, and has an internal portion extending toward the first die pad, each of the second plurality of leads corresponds to the external portion of one of the first plurality of leads.

14. The semiconductor packaging structure as claimed in claim 10, wherein the upper lead frame and the lower lead frame each further has a metal film electroplated thereon.

15. The semiconductor packaging structure as claimed in claim 10, wherein the cover is a transparent cover.

16. The semiconductor packaging structure as claimed in claim 10, wherein the cover is a metal cover.

17. The semiconductor packaging structure as claimed in claim 13, wherein the cover is a transparent cover.

18. The semiconductor packaging structure as claimed in claim 13, wherein the cover is a metal cover.

19. A semiconductor packaging structure comprising:

a metal lead frame having a die pad and having a plurality of leads arranged around the die pad, wherein the metal lead frame has multiple gaps and each gap is defined by an adjacent two of the plurality of leads, and the multiple gaps are filled with an isolating resin;

a wall portion formed on the metal lead frame and positioned along a periphery of the metal lead frame;

a chip mounted on the die pad of the metal lead frame and electrically connected to the plurality of leads; and

a transparent resin putted inside the wall portion to enclose the chip inside the wall portion.

20. The semiconductor packaging structure as claimed in claim 19 further having multiple notches and each notch is defined on a bottom surface of the metal lead frame and is communicated with one of the multiple gaps, wherein each notch and gap are filled with the isolating resin.